Integration & Validation of eFPGA for Physical Designers

Flex Logix

ABSTRACT

1. Introduction to embedded FPGA – what is it and value proposition.

2. EFLX embedded FPGA Gen2 Architecture in TSMC 16FFC/FF+

a. EFLX-100: 96 LUTs, 224 inputs, 224 outputs in 0.05mm2 with 5 routing metal layers so compatible with almost all FF+/FFC metal stacks

i. Arrays up to 5x5 or ~2500 LUTs with 25 intermediate sizes

b. EFLX-2.5K: 2520 LUTs, 2520 LUTs, 632 inputs, 632 outputs in 1.0mm2 with 6 routing metal layers so compatible with almost all FF+/FFC metal stacks

i. Arrays up to 7x7 or ~122.5K LUTs with 50 intermediate sizes

ii. DSP option replaces some LUTs with 40 MACs (22x22 multiply, pre-adder and accumulator

c. Gen2 features

i. 6-input LUTs for higher density and higher performance

ii. faster interconnect network especially for very large arrays

iii. MACs are pipelined 10 across for higher speed filters

iv. DFT >98% stuck-at fault coverage with vectors provided

v. Special test mode for ~100x test time improvement

Readback circuitry enables checking and correction of soft errors for high-reliability applications

1. Integration of EFLX embedded FPGA for Physical Designers

The following deliverables will be provided to enable integration of the embedded FPGA into the SOC

1. Validation of EFLX embedded FPGA - the architecture of validation chips to enable test at >1GHz with precise control of temperature and voltage will be described; test results of stress tests, building blocks and typical customer Verilog programs will be presented for typical and worst case T/V silicon measurements.

flexlogix Technologies, Inc.

Integration & Validation of eFPGA for Physical Designers

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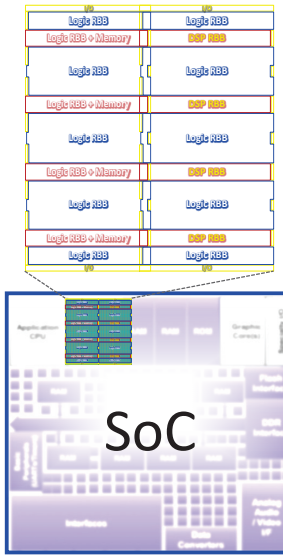
Agenda

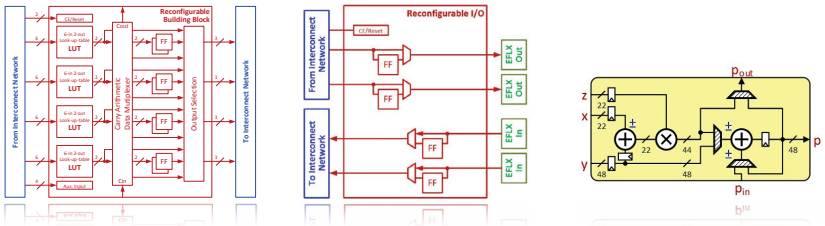
- Flex Logix EFLX Overview
- Gen2 Architecture Details Update
- SoC Integration Design Flow Discussion
- Validation of EFLX™ eFPGA Cores

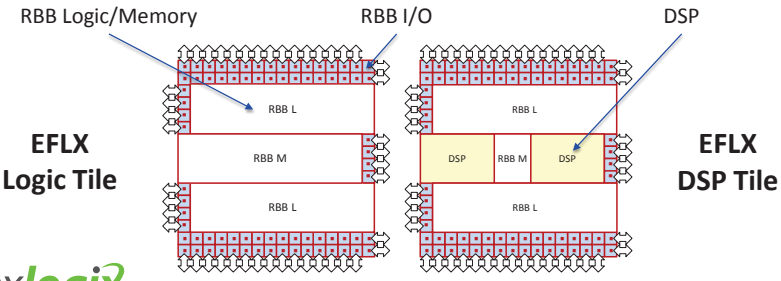


Why Put an FPGA in Your SoC?

- Reconfigure critical RTL
  - Changing standards
  - Changing algorithms
- Reconfigurable accelerators
- Reconfigurable data/control-path
- IO Flexibility

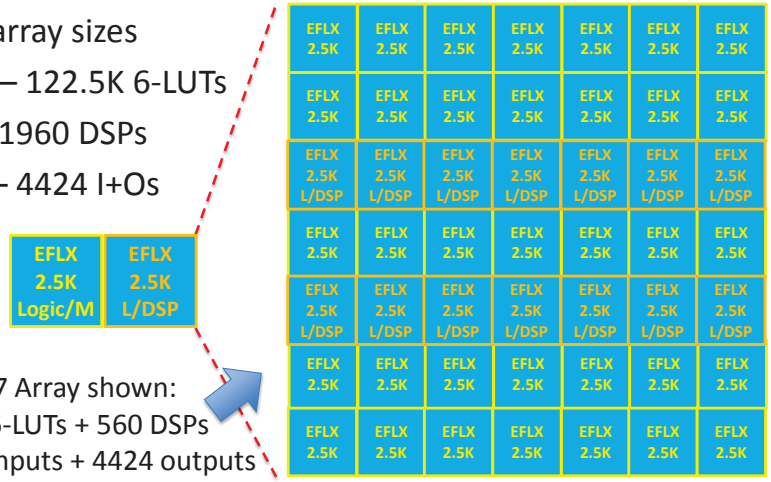
3 Reconfigurable Building Blocks (RBBs) in a Programmable Interconnect Network





EFLX-2.5K can tile up to 7x7

- >50 array sizes
- 2.5K – 122.5K 6-LUTs
- 40 – 1960 DSPs
- 632 – 4424 I+Os



7x7 Array shown:
115K 6-LUTs + 560 DSPs
4424 inputs + 4424 outputs

~50% Logic/DSP capacity of Kintex UltraScale+ XCKU3P
But **29x** the number of I/Os!

EFLX Availability – Customers Drive

	EFLX-100 Logic	EFLX-100 DSP	EFLX-2.5K Logic	EFLX-2.5K DSP
T 40 ULP/EF/LP	SILICON PROVEN	SILICON PROVEN	-	-
T 28HPM /HPC/HPC+	-	-	SILICON PROVEN	SILICON PROVEN
T 16FF+ T 16FFC	SILICON PROVEN	-	IN VALIDATION	IN VALIDATION

EFLX 2nd Generation Architecture

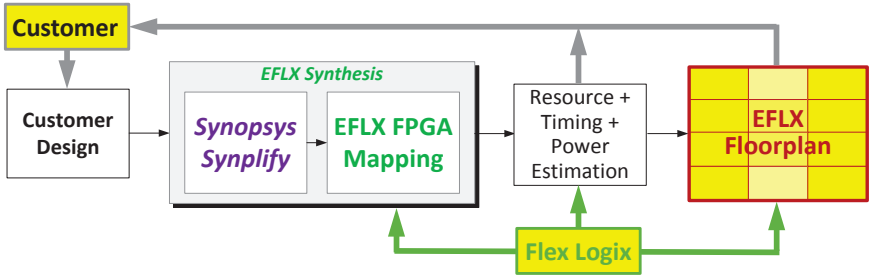
- Superior performance, logic density, & testability
  - Improved interconnect: faster routing & better logic utilization
  - Low skew, latency clock mesh with multiple inputs on all sides
- Optimized for wide, fast control logic
  - ~1GHz for single stage logic, SVT+LVT (TSMC 16FFC)
  - Four 6-input LUTs
  - 8 FF's with dedicated sync. set/reset
  - Concatenable 4-bit carry chain
  - Efficient RAM & shift-register logic
- Improved test coverage + significantly improved test time
  - 98.5% + ATPG coverage
  - Functional and at-speed (AC scan) scan supported

EFLX Design Considerations:
SoC Integration

EFLX IP: Performance, Resource/Floorplan Specification

Customer

Synthesizes RTL to estimate Performance, resources and specify floorplan



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Provides EFLX IP (GDS, LIB, LEF, etc.) for customer's floorplan

Power Analysis for Sign-Off

- Power analysis: Using dynamic vector-based simulations
  - Must have high LUT utilization, high freq. & high activity factor (AF)
  - Leakage quantified @ FFG(NP), 125°C, V_{DD}+10%

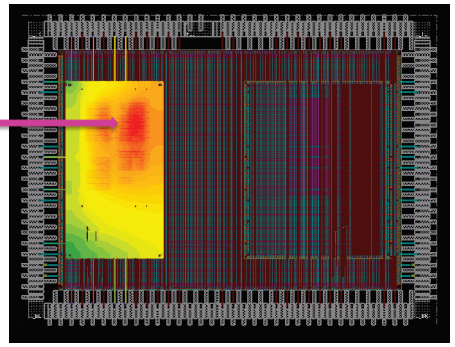
Dynamic Vector -based Voltus Simulation Results LUT Utilization 96%	TT 0.8V 85°C	FFGNP 0.88V 0°C	FFGNP 0.88V 125°C
Total Dynamic Power (mW) **sum (A+B+C)**	38.1	40.91	83.22
Internal (mW) **(A)**	12.11	11.06	40.16
Leakage (mW) **(B)**	1.35	0.17	12.66
Switching (mW) **(C)**	24.63	29.6	30.39

From Voltus simulations of EFLX-100 in TSMC 16FF+, with 96% LUT utilization at 800 MHz, for 22 cycles

IR Drop Analysis for Sign-Off

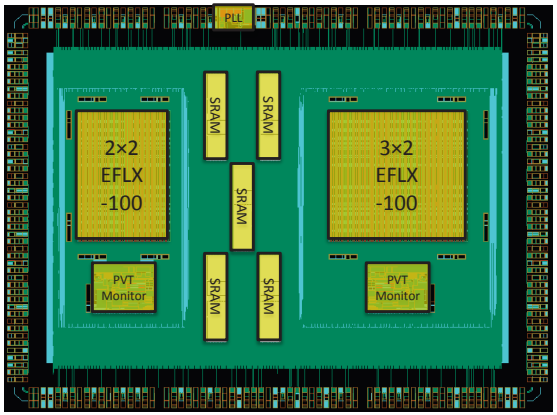
2x2 EFLX

- 6.1% Total IR (DC +AC) drop @1.0GHz inside the EFLX IP @ FFGNP, 0.88V, 125C



Validation of **EFLX eFPGA**

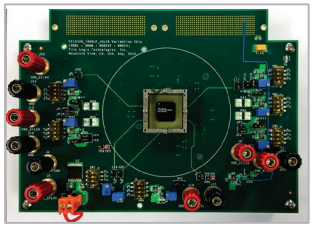
EFLX-100 16FF+ Validation Chip



- 2 EFLX-100 FPGA cores
  - 16FF+
  - Dense M4/M5/M6 power grid
- 5 dual ported 1K × 72 SRAM
  - Used to test EFLX ↔ SRAM
  - Pattern generator/checker
- 2 PVT* monitors
  - Measures on-die Process, Voltage, Temperature
- 1 on-chip PLL* – 1-3 GHz

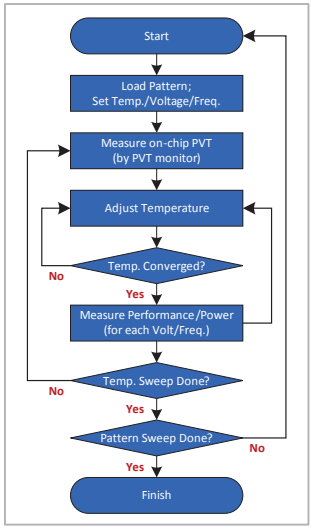
*PLL & PVT Monitor from Analog Bits (OIP Member)

eFPGA Automated Validation Platform



T16FF+ EFLX-100 Chip

Validation Setup



Software Platform: controls validation setup to characterize EFLX-100 IP

EFLX eFPGA
Silicon Measurement & Correlation

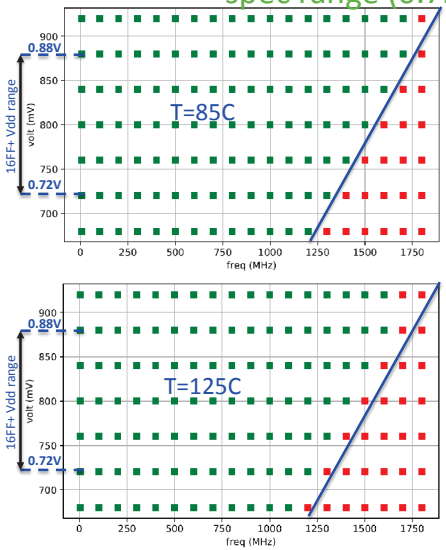
eFPGA EFLX-100 16FF+ (Performance) Simulation vs. Silicon

EFLX Compiler Performance results provide conservative targets vs. measured silicon

Test Case	eFPGA Util. (%)	# Logic Stages between FF	EFLX Compiler Simulated W.C. (MHz)		Silicon Measured* TT (MHz)	
			SSGNP V_j=0.72V, T_j=125C	TT V_j=0.8V T_j=85C	V_j=0.8V T_j=85C	V_j=0.8V, T_j=125C
Single Stage Control Logic	88.5	1	987	1470	1500	1400
Network Packet Inspection Block	87.5	2	560	834	900	800
EFLX_to_SRAM	92.7	2	483	719	900	800
16 bit-Multiplier with PRBS gen/checker	87.5	10	217	329	500	400

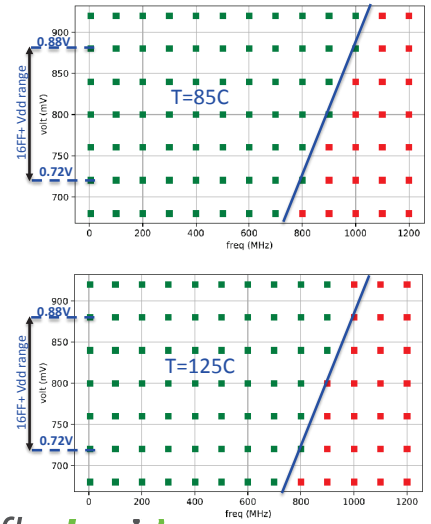
*measured frequency shmoo 100MHz delta

Shmoo of Single Stage- Performance beyond valid voltage spec range (0.72V – 0.88V)



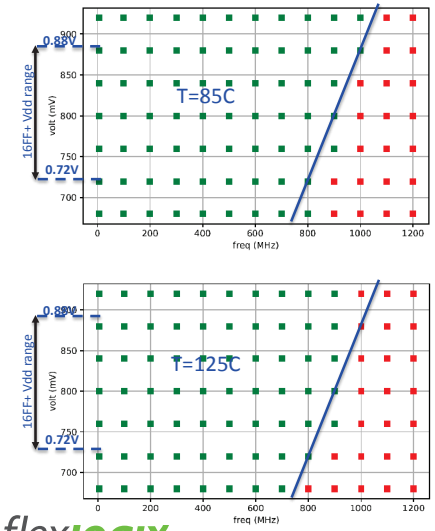
2x2 Array
- 88.5% eFPGA Utilization
- 900MHz @ Vj = 0.8V, Tj=85C

Shmoo of Network Packet Performance beyond valid voltage spec range (0.72V – 0.88V)



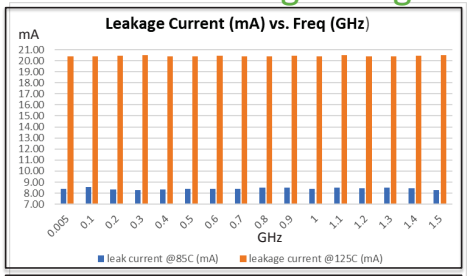
2x2 Array
- 87.5% eFPGA Utilization
- 1.5GHz @ Vj = 0.8V, Tj=85C

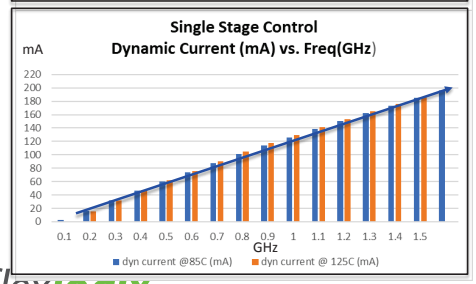
Shmoo of EFLX-to-SRAM Performance beyond valid voltage spec range (0.72V – 0.88V)



2x2 Array
- 92.7% eFPGA Utilization
- 900MHz @ Vj = 0.8V, Tj=85C

Leakage/Dynamic Current Measurement Results for Single-Stage Control Logic



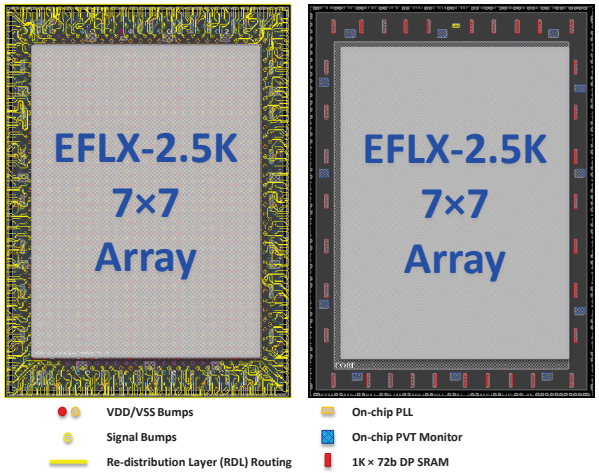


Temp	Leakage Current (mA)	
	Simulated	Measured
85C	6.7*	8.4*
125C	22.8**	20.4*

*Voltus simulated (TSMC 9T std. cell library)
**TSMC spice model ~3.4x increase in leakage (85C→125C)

Dynamic current increase linearly with frequency

EFLX-2.5K 16FFC– In Validation Now



- 7x7 array of EFLX 2.5K cores
  - 35 Logic core
  - 14 DSP cores
- 42 dual ported 1K × 72 SRAM
- 12 PVT monitors
- 1 on-chip PLL – 1-3GHz
- 70 mm^2 total
  - <49mm^2 for EFLX core

Summary of 16FFP/16FFC

- FlexLogix has silicon proven eFPGA EFLX-100 in 16FFP/16FFC
- IP is fully functional across a 4+ RTL applications across 2x2 and 3x2 Arrays
- Larger EFLX-2.5K Logic/DSP Core in Validation now
- High Performance for Accelerators, Packet Inspection, Machine Learning and ANY RTL that required reconfigurability post fabrication

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